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NOV 0 3 2006

Amendments to the Claims

Please amend the claims as follows:

1. (Currently Amended) A method of forming a trench in a semiconductor device, comprising:

forming a polish stop layer on a semiconductor substrate;

forming an organic anti-reflection coating on the polish stop layer;

selectively etching the anti-reflection coating to form an anti-reflection coating pattern;

etching the polish stop layer and the semiconductor substrate ~~to a predetermined depth to form a trench~~ such that ends of the polish stop layer adjacent to the trench are rounded along substantially the entire thickness of the polish stop layer, and ~~the~~ a trench ~~has~~ having sloped sidewalls is formed to a predetermined depth; and

forming an insulation layer that fills the trench.

2. (Currently Amended) The method of claim 1, wherein etching the polish stop layer ~~and the semiconductor substrate~~ comprises injecting one or more of CHF_3, CF_4, O_2, HeO_2, and Ar, creating a plasma and dry etching the polish stop layer ~~and the semiconductor substrate~~.

3. (Currently Amended) The method of claim 2, wherein etching the polish stop layer ~~and the semiconductor substrate~~ comprises injecting at most 60sccm of CHF_3, gas, at most 60sccm of CF_4 gas, at most 30sccm of O_2 gas, at most 60sccm of HeO_2, gas, and at most 200sccm of Ar gas.

4. (Previously presented) The method of claim 2, wherein creating a plasma comprises applying 50-500W of power while injecting one or more of CHF_3, CF_4, O_2, HeO_2, and Ar.

5. (Currently Amended) The method of claim 2, further comprising creating a pressure environment of 5-100mTorr during etching the polish stop layer ~~and the semiconductor substrate~~.

6. (Currently Amended) The method of claim 1, wherein an area of the polish stop layer exposed through the antireflection coating pattern is etched ~~to form the trench~~, and ends of the anti-reflection coating pattern are also etched such that the ends of the anti-reflection coating are rounded.

7. (Not entered)

8. (Currently Amended) The method of claim 6, wherein etching the polish stop layer ~~and the semiconductor substrate~~ comprises injecting one or more of CHF_3, CF_4, O_2, HcO_2, and Ar, creating a plasma and dry etching the polish stop layer ~~and the semiconductor substrate~~.

9. (Currently Amended) The method of claim 8, wherein etching the polish stop layer ~~and the semiconductor substrate~~ comprises injecting at most 60sccm of CHF_3 gas, at most 60sccm of CF_4, gas, at most 30sccm of O_2 gas, at most 60sccm of HcO_2 gas, and at most 200sccm of Ar gas.

10. (Previously presented) The method of claim 8, wherein creating a plasma comprises applying 50-500W of power while injecting one or more of CHF_3, CF_4, O_2, HcO_2, and Ar.

11. (Currently Amended) The method of claim 8, further comprising creating a pressure environment of 5-100mTorr during etching the polish stop layer ~~and the semiconductor substrate~~.

12. (Previously presented) The method of claim 1, wherein the polish stop layer has a thickness of 1000-3000Å.

13. (Previously presented) The method of claim 1, wherein the polish stop layer comprises a material that is more slowly polished than an insulation material of the insulation layer.

14. (Previously presented) The method of claim 13, wherein the polish stop layer comprises a silicon nitride layer having a thickness of 1000-3000Å.

15. (Currently Amended) The method of claim 14, wherein etching the polish stop layer ~~and the semiconductor substrate~~ comprises injecting one or more of CHF_3, CF_4, O_2, HeO_2, and Ar, creating a plasma and dry etching the polish stop layer ~~and the semiconductor substrate~~.

16. (Currently Amended) The method of claim 15, wherein etching the polish stop layer ~~and the semiconductor substrate~~ comprises injecting at most 60sccm of CHF_3, gas, at most 60sccm of CF_4 gas, at most 30sccm of O_2 gas, at most 60sccm of HeO_2, gas, and at most 200sccm of Ar gas.

17. (Previously presented) The method of claim 15, wherein creating a plasma comprises applying 50-500W of power while injecting one or more of CHF_3, CF_4, O_2, HeO_2, and Ar.

18. (Currently Amended) The method of claim 15, further comprising creating a pressure environment of 5-100mTorr during etching the polish stop layer ~~and the semiconductor substrate~~.

19. (Previously presented) The method of claim 1, wherein forming the insulation layer comprises forming the insulation layer to cover the polish stop layer and inner walls of the trench, and chemical-mechanical polishing the insulation layer until the polish stop layer is exposed.

20. (Previously presented) The method of claim 1, wherein prior to forming the insulation layer, the method further comprises forming a liner oxidation layer on the polish stop layer and the trench, and forming the insulation layer comprises depositing an insulation layer material on the liner oxidation layer such that the trench is filled with the insulation layer material.

21. (New) The method of claim 1, further comprising depositing a pad oxidation layer on the semiconductor substrate, wherein the polish stop layer is deposited on the pad oxidation layer.

22. (New) The method of claim 21, wherein etching the polish stop layer and the semiconductor substrate further comprises etching the pad oxidation layer.